Approach for a comprehensive definition of the electrical interface between HVDC converter and cable

Simon **BECKLER**, Jörg **REISBECK**, Florian **EXL**, TransnetBW (Germany)
s.beckler@transnetbw.de, j.reisbeck@transnetbw.de, f.exl@transnetbw.de
Fabian **SCHELL**, Fichtner, (Germany), fabian.schell@fichtner.de

ABSTRACT

For high voltage direct current (HVDC) projects, it is important to describe the electrical interface between converter and cable system thoroughly. The interface in this respect is defined by continuous and transient voltage and current parameters. The actual stress levels and wave shapes occurring in an HVDC cable system differ from standard test parameters. In this paper, a set of parameters is derived based on the analysis of occurring transients utilizing electromagnetic transient (EMT) simulations. Since the stress levels depend on both cable system and converter design, an iterative procedure to derive project specific values is proposed.

KEYWORDS

Extruded cable; converter; VSC HVDC; electrical interface; voltage stress; transients

INTRODUCTION

Most HVDC systems in the past decades have been realized with overhead line or mass-impregnated (MI) cables. Extruded cable systems have benefits regarding cost and environmental impact over MI cables. However, HVDC systems used with line-commutated converters (LCC) require a voltage polarity reversal in order to change power flow direction, which is a challenge for extruded cables.

With the commercial introduction of HVDC systems based on voltage source converters (VSC) in half-bridge (HB) modular multilevel converter (MMC) topology, e.g. the Trans-Bay cable project in 2010 [1], extruded DC cable systems have gained increasing interest, since polarity reversal is no longer required to change the power flow direction.

VSC technology is developing at a rapid pace. Available voltage levels and active power capacity are increasing and new technologies such as full-bridge (FB) MMC (only considered for overhead line transmission so far) are already in the realization stage. Furthermore, MMC-projects in bipolar (see [2]) and rigid bipolar configuration (see [3]) as well as mixed overhead line – cable systems will be built. Based on this progress, further developments can be expected in the near future.

Extruded cable technology can be used for all these configurations. However, each configuration causes different electrical stresses for the cable. And the available test practices (see e.g. [4], [5]) are either not applicable for all relevant voltage levels or it is not clear, if the given recommendations and standards cover all the transient stresses observed in the actual HVDC systems.

Therefore, and in order to cover all the relevant stresses independently of the actual HVDC system configuration, a *comprehensive electrical interface* is required that contains the relevant parameters to describe the occurring stresses.

This electrical interface is especially relevant when HVDC converter and cable system are sourced independently. In this case, a procedure is required to derive the values for the considered parameters.

Furthermore, this electrical interface definition can be a valuable input to a further development of HVDC cable test practices.

In this paper, a procedure for such an electrical interface definition is introduced and several typical values are given for an illustrative example. Also, an iterative design procedure is proposed that enables derivation of the relevant parameters on a project specific base.

ELECTRICAL INTERFACE DESCRIPTION

Voltage requirements and testing

The relevance for a thorough analysis and determination of continuous and transient voltage stresses results from insulation coordination principles. In 2001, Cigré JWG 21/33 studied the matching of the required withstand capabilities with actual service requirements for AC underground cable systems [6], however, focusing primarily on cost reduction at that time.

Furthermore, the importance and correlation between ageing aspects, characterized by the “lifetime curve”, and actual overvoltage stresses in the network has been pointed out therein (see Figure 1).

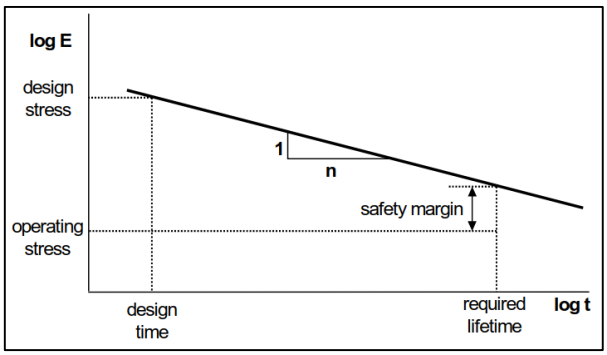

Figure 1 – Typical lifetime curve for cables with extruded insulation (AC and DC) [6]

Like in all subsequent IEC standards for AC and DC cables with extruded insulations, the continuous withstand voltage tests are expressed by *multiplication factors* for the “design voltage” U_0 and a duration.

Furthermore, a safety margin between design stress and operating stress is recommended, to account for the consumption of lifetime during routine, sample and type testing. Finally, a long term “pre-qualification test” (long-term test) has been postulated in [6] as a pre-requisite for

future EHV cable systems to simulate an expected lifetime of 40 years.

Nevertheless, the testing "philosophy" composed of

- *continuous* withstand voltage levels and
- *transient* voltage stresses
  (i.e. standard switching and lightning impulse),

as implemented later in all recommendations and standards also for extruded DC cables (see [4], [5]), can be considered as insufficient to account for the entirety of voltage stresses that extruded DC cables can be subjected to in actual HVDC schemes, particularly for transient voltage stresses, both in amplitude and duration, as explained hereafter.

Actual electrical stresses in HVDC systems

Continuous voltage stresses

The rated DC voltage U_0 is defined in the standard as the "voltage between conductor and metal screen or sheath for which the cable system is *designed*" [4]. From the design perspective it is used to determine the voltage test levels as explained above.

On the other hand, the rated voltage U_0 can also be used to determine continuous operational voltage ranges, including a maximum system voltage.

In actual HVDC systems it is impossible to produce a constant DC voltage without variations. Due to ripple, harmonics, imbalances and measuring tolerances the *maximum* continuous voltage will always be higher than the rated (nominal) DC voltage. Following the approach of producing DC test voltages under laboratory conditions, the ripple content shall not be greater than 3% according to [4]. The same value can be applied here to determine the ripple content to be added to U_0 (RMS value).

However, if following the principles of [7] an approximate 2% shall be considered for measurement tolerances on top of that (Peak value). Thus, the resulting maximum voltage that the cable system must be able to withstand *continuously* is approximately 5% higher than the rated voltage U_0. And that is finally the *continuous* voltage level U_{max} that the cable system is expected to withstand for its entire lifetime. Transient voltage stresses, to be accounted for on top of that, are discussed in detail later.

The chosen way of determining U_{max} from U_0 by adding contingencies for clearly defined components can be described as "bottom-up" approach. According to recent project experience the determination of the *design* voltage U_0 requires clarification, however.

In 2017 Cigré published the Technical Brochure No. 684 on "Recommended Voltages for HVDC Grids" [8], in which the "rated voltage of cable" U_0 is derived from a system view (see Figure 18 therein). Major confusion has been created during the course of a recent project specification however, by introducing two almost identical designations for maximum voltages:

Starting from a "maximum continuous (system) *operating* voltage" a contingency range of 2 to 5%, as given in [8], is added for harmonics, ripples and measuring tolerances to obtain the "maximum continuous voltage", with the latter being equal to the "rated voltage of cable" U_0. This mismatch is explained by the example shown in Table 1 for nominal voltage of 320 kV.

Table 1 – Example of different interpretations of U_0

Actual practice (recommended)		Following [8]
Maximum system voltage (= withstand level)	336 kV	
Harmonics, ripple, measurement tolerances	+5%	
Rated design voltage (U_0), Basis for voltage test levels	320 kV	Rated voltage of cable (U_0) incl. harmonics, ripple etc.
	+5%	Harmonics, ripple, measurement tolerances
	304.8 kV	Maximum continuous operating voltage
	<300 kV	Nominal system voltage (thus significantly lower)

Focusing on the resulting system voltages only (304.8 kV versus 336 kV), it becomes clear that the actual practice creates a wider range of operation, thus allowing for a better use of the cable systems designed in accordance with the current standards.

Furthermore, it is of utmost importance to have a clearly defined basis for the determination of all test voltage levels (U_0 in left column); and on top of that, to maintain the validity of existing pre-qualification and type tests according to the range of approval described in [4] and [5].

Finally, it can be stated that, in order to avoid misunderstandings and consequential faults when defining the design voltages of the HVDC interface, it is recommended to verify and agree upon a common U_0 value, both by designation and value, to be used as the basis for steady-state test and design voltages.

Transient stresses

HVDC cable systems are exposed to current and voltage stresses caused by dynamic and transient events that might occur over the lifecycle of the HVDC system. The following events can lead to transients that will be observed by the cable system:

- Faults on the DC side
- Faults within the converter station
- Dynamic events on the AC side (e.g. AC fault ride through)
- Switching (e.g. grounding of DC pole)

The different types of transients result in completely different transient characteristics. In [9], it is shown that for a symmetrical monopolar configuration a pole to ground fault leads to overvoltages on the healthy pole as well as well as polarity reversals at the faulted pole.

A transient event causes different stresses seen at different locations within the cable system. Figure 2 and Figure 3 show the occurring transients for a DC pole to ground fault close to the converter station of an HVDC system in symmetrical monopolar configuration with 200 km length. The transients are shown for different measurement points along the cable system. It should be noted that only an illustrative example is shown. The actual occurring values might be considerably higher than the values shown in this paper.

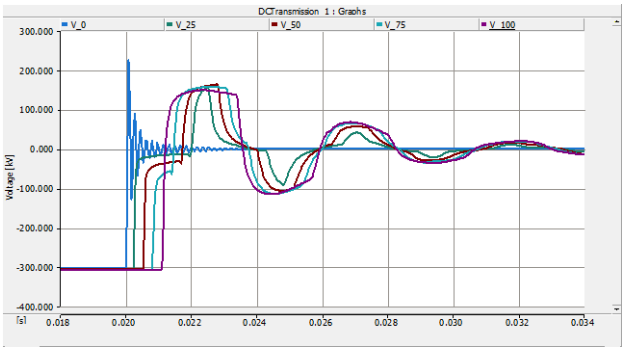

Figure 2 – Voltages at faulted pole during pole to ground fault at different measurement points (0%, 25%, 50%, 75%, 100%) of cable system length

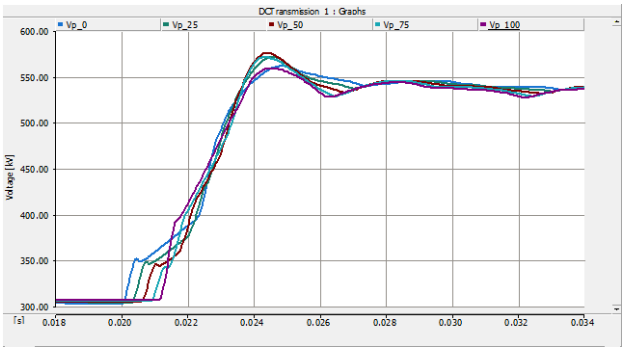

Figure 3 – Voltages at healthy pole during pole to ground fault at different measurement points (0%, 25%, 50%, 75%, 100%) of cable system length

Especially for the faulted pole completely different characteristics for different measuring locations can be observed in Figure 2. At 0% of the cable system length (i.e. close to the fault) high frequency oscillations occur (frequency of around 5.6 kHz). The peak value of the polarity reversal is quite high, reaching around -0.8 p.u. For measurement locations along the cable route the peak value and oscillating frequency are less. However, a larger voltage-time-integral of the opposite polarity can be observed. A general explanation of the fault behavior is provided e.g. in [9] and [10].

The characteristic of the overvoltages at the healthy pole in Figure 3 shows a time-to-peak of around 3 ms and a time-to-half that can amount up to several seconds. Therefore, a significantly different characteristic compared to standard test shapes can be observed. In [11], it is analyzed if these wave shapes can be tested with different-than-standard impulse waveforms. Furthermore, the HVDC system configuration and converter topology will have an impact on the occurring transients. E.g. in [12], overvoltages for a rigid bipolar configuration are analyzed.

It is important to capture that the occurring transients in an HVDC system are quite diverse and appear different to standard test shapes. Therefore, in order to discuss the transient stresses between converter manufacturers, cable manufacturers and HVDC system owners, it is required to derive a common language or a standardized form that helps categorize those transients independently of the actual system and project specific design.

Therefore, based on a variety of HVDC configurations, the authors propose a parameter set that can describe the occurring transients in a real HVDC system.

Electrical interface parameter set

A crucial step in the specification of requirements regarding insulation co-ordination and current loads is the definition of representative values. Hereafter, the derivation of the electrical interface parameter set is described for voltage parameters. A similar procedure can be applied for current parameters.

To structure the parameter set a general categorization of the phenomena is required. IEC 60071-1 describes a categorization for the well-known AC voltage phenomena based on defined parameters (e.g. frequency, time to peak, time to half value). Furthermore, the categories are assigned to standardized withstand voltages.

In some cases, as highlighted in the previous section, the occurring transients could not be clearly assigned to the given categories or the general shapes differ vastly from these categories. Therefore, some adaptions and additions have been implemented.

Table 2 shows the derived general categorization, based on IEC 60071-1. In order to account for the stresses observed in real systems (see e.g. Figure 2 and Figure 3) new categories have been added, namely very slow front transient overvoltages and oscillating polarity reversals.

Table 2 – general categorization of voltage phenomena based on IEC 60071-1

Category		Parameters	
low frequency	continuous voltage	frequency	f = 0 Hz
		duration	≥ 3600 s
	temporary overvoltage	frequency	f ≥ 0 Hz
		duration	0,02 s ≤ T_t ≤ 3600 s
transient	very slow front overvoltage	time to peak	T_P > 500 µs
		time to half value	T_2 > 20 ms
	slow front overvoltage	time to peak	20 µs < T_P ≤ 5000 µs
		time to half value	T_2 ≤ 20 ms
	fast front overvoltage	time to peak	0,1 µs < T_P ≤ 20 µs
		time to half value	T_2 ≤ 300 µs
	very fast front overvoltage	time to peak	T_P ≤ 100 ns
		frequency component (high frequency)	0,3 MHz < f_1 < 100 MHz
		frequency component (base frequency)	30 kHz < f_2 < 300 kHz
Oscillating polarity reversals	low frequency	frequency	f ≤ 1 kHz
	high frequency	frequency	f > 1 kHz

Between categories “very slow front overvoltage” (VSFO) and “slow front overvoltage” (SFO) exists an intended overlap within the parameter “time to peak” (T_P > 500 µs for VSFO and T_P ≤ 5000 µs for SFO). The distinction is made solely by the “time to half values” (T_2 > 20 ms for VSFO and

T_2 ≤ 20 ms for SFO). The parameters for SFO follows strictly the IEC 60071-1 definition. The parameter T_P for VSFO has been defined with the aim to include all "long-tail-overvoltages" (T_2 > 20 ms) with values for T_P that are double the virtual front duration of the standardized switching impulse (T_P = 250 µs) within the VSFO category.

Furthermore, to achieve a comprehensive definition of the occurring stresses, additional parameters have been specified within the general categories. Table 3 shows the proposed set of parameters needed to achieve a comprehensive characterization of the observed voltage stresses.

An essential aspect for each category is the distinction between stresses with the same polarity or with opposite polarity regarding the designated polarity. For each case, different or additional parameters could be important.

For example within the continuous voltage category, the base parameter set for the stresses with designated polarity and opposite polarity are similar. However, recommended resting times and the maximum approved operating time are important additional parameters to assess the benefit of an operation with opposite polarity.

Table 3 – comprehensive description of occuring voltage stresses based on the general categorization

Category and parameter	Unit
Comprehensive overvoltage characteristics	
Continuous voltage	
Designated polarity	
Peak value	kVp
DC component	kV_{DC}
RMS value	kV_{RMS}
Harmonic content for all integer frequencies	kV_{RMS}
Opposite polarity	
Peak value	kVp
DC component	kV_{DC}
RMS value	kV_{RMS}
Harmonic content for all integer frequencies	kV_{RMS}
Duration until polarity reversal after grounding (resting time, grounded, at ambient temperature)	h
Duration of operation at opposite polarity	s/min/h
Temporary overvoltages	
Peak value	kVp
DC component	kV_{DC}
RMS value	kV_{RMS}
Duration of maximum value	ms
Very-slow-front overvoltages (time to peak > 500 µs)	
Same polarity	
Time to peak	µs
Maximum gradient (over all cases)	kV/ms
Maximum gradient (for the case leading to maximum peak value)	kV/ms
Peak value	kVp
Settling time to 90% of peak value	ms
Settling time to rated voltage	s
Opposite polarity	
Time to peak (from U_0 to opposite polarity peak value)	µs
Maximum gradient (over all cases)	kV/ms
Maximum gradient (for the case leading to maximum peak value)	kV/ms
Maximum value (peak – peak)	kVp
Peak value (opposite polarity)	kVp
Maximum integral voltage-over-time after fault occurrence (first peak only, opposite polarity only)	kVs
Duration of peak value at opposite polarity	ms
Slow-front overvoltages (20 µs < time to peak < 5000 µs)	
Same polarity	
Time to peak	µs
Time to half	µs
Peak value	kVp
Opposite polarity	
Time to peak (from U_0 to opposite polarity peak value)	µs
Time to half	µs
Peak value	kVp
Fast-front overvoltages (0,1 µs < time to peak < 20 µs)	
Same polarity	
Time to peak	µs
Maximum gradient	kV/µs
Time to half	µs
Peak value	kVp
Opposite polarity	
Time to peak (from U_0 to opposite polarity peak value)	µs
Maximum gradient	kV/µs
Time to half	µs
Peak value	kVp
Very-fast-front overvoltages (if applicable) time to peak < 0,1 µs	
Same polarity	
Time to peak	ns
Maximum gradient	kV/ns
Time to half	µs
Frequency content with more than 5% U_0	kV
Peak value	kVp
Opposite polarity	
Time to peak (from U_0 to opposite polarity peak value)	ns
Maximum gradient	kV/µs
Time to half	µs
Frequency content with more than 5% U_0	kV
Peak value	kVp
Oscillating polarity reversal with high frequency (frequency > 1 kHz)	
Frequency	Hz
Maximum gradient	kV/µs
Peak value during polarity reversals	kVp
Maximum voltage difference during polarity reversals	kV
Maximum integral voltage-over-time after fault occurrence (first peak only, opposite polarity only)	kVµs
Maximum integral voltage-over-time after fault occurrence (opposite polarity only)	kVµs
Number of polarity reversals until U_{dc} < 5% U_0 for oscillating polarity reversals	-
Duration until U_{dc} < 5% U_0 for oscillating polarity reversals	ms
Oscillating polarity reversal with low frequency (frequency < 1 kHz)	
Frequency	Hz
Maximum gradient	kV/µs
Peak value during polarity reversals	kVp
Maximum voltage difference during polarity reversals	kV
Maximum integral voltage-over-time after fault occurrence (first peak only, opposite polarity only)	kVs
Maximum integral voltage-over-time after fault occurrence (opposite polarity only)	kVs
Number of polarity reversals until U_{dc} < 5% U_0 for oscillating polarity reversals	-
Duration until U_{dc} < 5% U_0 for oscillating polarity reversals	ms

Further parameters defined additionally to IEC 60071-1 categorization are:

- Different gradients
  E.g. to distinguish between the maximum gradient in total over all observed transients or the gradients for particular events
- Different peak values
  E.g. for transient polarity reversals, to distinguish

between maximum peak to peak values or maximum total values for the opposite polarity
- Voltage-time-integrals
  E.g. to compare frequent polarity reversals
- Different decay rates
  E.g. to describe different phases within the slow front overvoltage events
- Different frequency components
  E.g. to describe ripple, coupling and control impacts within the continuous voltage category, to describe resonance phenomena within the transient and frequent polarity reversal events

In order to support the understanding of the individual parameters, illustrations by means of simulated wave shapes or temporary overvoltage (TOV) curves are recommended similar to the examples shown in this paper.

Not all categories are necessarily applicable for all HVDC projects. E.g. for systems comprising of 100% cables without gas-insulated switchgear on the DC side, fast-front and very-fast-front transients might not occur. Therefore, the respective parameters can be left blank.

The introduced parameter set should not be mistaken for newly developed test levels or shapes but rather support the discussion between all relevant parties in order to match cable system design and testing with the actual stresses in a real HVDC system.

Example of application

Figure 3 is used to derive the values for the newly defined category "*very slow front overvoltage with same polarity*".

The values of this category are determined by analyzing the wave shapes. In Table 4 some values for this illustrative example are summarized.

Table 4 – Determined values for very-slow-front overvoltages according to illustrative example

Very-slow-front overvoltages (time to peak > 500 µs)	
Same polarity	
Time to peak	3000 µs
Maximum gradient (over all cases)	96 kV/ms
Maximum gradient (for the case leading to maximum peak value)	166 kV/ms
Peak value	577 kVp
Settling time to 90% of peak value	42 ms
Settling time to rated voltage	unknown

It can be observed that the time to peak and the peak value do not directly correspond to the maximum gradient. Furthermore, the maximum gradient for the case with the highest overvoltage (Vp_50) is lower than the maximum gradient observed for all considered cases (Vp_100). In this example, only different fault locations are considered. The maximum gradient might as well appear for a completely different fault scenario. Furthermore, the values will differ significantly with cable system length [10].

This is a typical case for the transient voltages at the healthy pole during pole to ground faults in symmetrical monopolar configurations. It is important to address, that the settling time to the rated voltage depends heavily on the post fault system configuration and intrinsic discharge of the cable system. Without active discharging, those times can reach up to several hours. The duration until the voltage drops to 90% of the peak-value is however only several ms.

In Figure 4 an example is given for the newly defined category "oscillating polarity reversals – low frequency". In this case, the V_100 measuring location as seen in Figure 2 is considered.

The wave shapes are analyzed and the values according to the category "*Oscillating polarity reversal with low frequency*" are derived. The results are summarized in Table 5.

Table 5 – Determined values for low frequency oscillating polarity reversal according to illustrative example

Oscillating polarity reversal with low frequency (frequency < 1 kHz)	
Frequency	224 Hz
Maximum gradient	2.3 kV/µs
Peak value during polarity reversals	149 kVp
Maximum voltage difference during polarity reversals	457 kV
Maximum integral voltage-over-time after fault occurrence (first peak only, opposite polarity only)	0.32 kVs
Maximum integral voltage-over-time after fault occurrence (opposite polarity only)	0.48 kVs
Number of polarity reversals until U_{dc} < 5% U_0 for oscillating polarity reversals	6
Duration until U_{dc} < 5% U_0 for oscillating polarity reversals	15-20 ms

Oscillating polarity reversals are typical transients occurring at the faulty pole during pole to ground faults. However, for both "oscillating polarity reversal" categories (low and high frequency) distinct typical values are difficult to determine since the values vary greatly for different measurement points as shown in Figure 2. Therefore, it should be considered in general to add tolerances to the determined values.

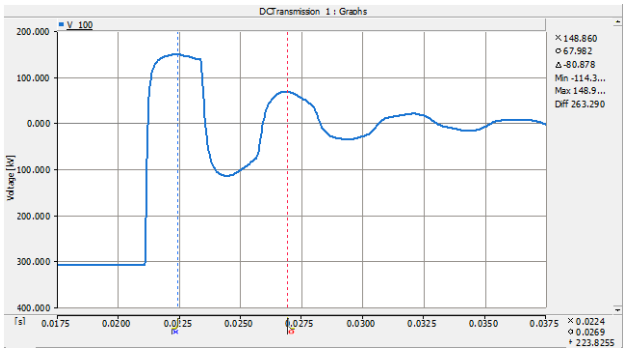

Figure 4 – Example for "oscillating polarity reversals with low frequency" (f ≈ 224 Hz)

ITERATIVE DESIGN PROCEDURE

This section deals with the challenges of deriving the project specific values of the electrical interface. Each HVDC system is unique and generally agreed upon or even standardized parameters are not available. This requires a defined procedure in order to describe the interface parameters and ensure technical compliance between converter and cable system.

It should be noted that the electrical interface values not only depend on the converter design but also on the

electrical properties of the DC cable. On the one hand, the cable system supplier requires information regarding the stress levels in order to assess the withstand capability of his cable system design. On the other hand, the converter supplier needs the electrical and geometrical cable design in order to derive those stress levels. This requires a strong coordination between the owner of the HVDC system, the cable supplier and the converter supplier, especially when these components are sourced separately. Therefore, an iterative design procedure is required which is especially challenging since a range of technical solutions by different cable system and converter suppliers are possible at early stages of an HVDC project.

As a starting point, initial values have to be defined, i.e. preliminary cable system information will be handed over to the converter suppliers and preliminary stress levels will be given to the cable system supplier. In order to account for the uncertainty at this early stage, rather a range than explicit values of preliminary information has to be defined. The range can be smaller, when the future HVDC system owner has conducted detailed studies prior to the technical specifications.

At the first iteration step, the converter supplier will calculate the stress levels based on his specific converter design and the preliminary cable designs while the cable supplier will consider the preliminary stress levels to derive the design for his cable.

The HVDC system owner aggregates and distributes the obtained results to the relevant parties. Therefore, for the next iteration step, more specific information can be used by converter and cable system supplier. After each iteration step, a coordination between all parties is required.

The final aim is to have robustly determined stress levels, which are confirmed by the cable supplier. This is a cumbersome task due to the large organizational effort required, but might be necessary to ensure technical compliance between converter and cable system. This procedure helps minimizing future project risks by identifying and mitigating the electrical interface problems.

CONCLUSION

The definition of an electrical interface between HVDC converter and cable system is a crucial part when specifying and designing an HVDC system. This paper presents an approach to derive such an interface definition in a comprehensive way. The approach involves three steps: clear definition of continuous (rated) voltage, definition of a comprehensive parameter set and a procedure to derive the values on a project specific base.

At first, the necessity for a clear definition of the rated cable voltage U_0 is highlighted to define the maximum continuous withstand voltage as well as the base voltage for cable system testing.

Secondly, an extended parameter set to define the electrical interface is defined based on the analysis of actual occurring stresses in a real system. An example of application is given and the values for two newly defined categories are given.

Finally, an iterative design procedure to derive the project specific values of the electrical interface is introduced that considers the information available for all relevant parties at different stages.

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